METHOD OF MANUFACTURING VERTICAL TRENCH MISFET

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FIELD OF THE INVENTION

The present invention relates to a vertical MISFET (field-effect transistor of a metal-insulator-semiconductor structure) used in a power source incorporated in electronics, or a power source for driving motors, for example, wherein the MISFET has trenches, and exhibits a high withstand voltage and a low ON-state resistance. The present invention also relates to a method of manufacturing such a vertical MISFET as described above.

BACKGROUND OF THE INVENTION

Among various power semiconductor devices, a power MOSFET (field-effect transistor of a metal-oxide-semiconductor structure) as one kind of MISFET is known for a relatively low power loss and high-speed switching. The MOSFET, however, is desired to have a reduced ON-state resistance, since this element having a single kind of carriers (electrons or holes) performs no modulation of its conductivity by introducing minority carriers. On the other hand, a technique for forming trenches in a surface of a semiconductor element finds various applications, for example, to reduce the ON-state resistance of the semiconductor element. Thus, various structures of semiconductor elements having trenches have been proposed in recent years.

FIG. **7**(*a*) is a cross sectional view showing a principal part of a conventional vertical MOSFET. This figure shows a unit cell of the MOSFET. In the actual MOSFET, this unit cell is repeatedly reversed with respect to the vertical line such that a multiplicity of unit cells are connected in series with each other. While this figure only shows an active region of the transistor assigned to perform switching of electric current, the actual semiconductor element needs to be provided with a peripheral portion which mainly contributes to withstanding voltage. The peripheral portion will not be described in detail since this portion is constructed in a normal form. In FIG. **7**(*a*), an n drain drift region **702** in the form of an n epitaxial layer is superposed on an n^+ substrate **701**, to provide a semiconductor substrate. A p base region **703** is formed in a selected area of a surface layer of the semiconductor substrate, and an n^+ source region **704** is formed in a part of a surface layer of the p base region **703**. A gate electrode **707** is formed, through a gate oxide film **706**, on the surface of the p base region **703** interposed between exposed surface areas of the n^+ source region **704** and the n drain drift region **702**. A source electrode **708** is formed in contact with both the n^+source region **704** and the p base region **703**, and a drain electrode **709** is formed on the rear surface of the n^+ substrate **701**. In operation of this semiconductor element, when a positive voltage is applied to the gate electrode **707**, an n-type inversion channel appears in a surface layer of the p base region **703** right below the gate electrode **707**, whereby the n^+ source region **704** is conducted with the n drain drift region **702**. When the transistor is in its OFF state in which the gate voltage is not higher than a threshold voltage, the n-type inversion channel does not appear in the surface of the p base region **703**. In this state, therefore, the voltage applied to the transistor is carried by a depletion layer which expands over both sides of a pn junction between the p base region **703** and the n drain drift region **702**.

In the power MOSFET, several millions of unit cells each having the structure of FIG. **7**(*a*) are integrated within one chip, so as to reduce the ON-state resistance. The ON-state resistance per unit area (Ron*A) and the withstand voltage are used as parameters for evaluating the performance of the power MOSFET. Where the withstand voltage is constant, the size of the chip is reduced with reduction of the ON-state resistance (Ron*A), so that the transistor can be manufactured at a reduced cost.

FIG. **7**(*b*) is a view explaining details of the ON-state resistance of the power MOSFET of FIG. **7**(*a*). The ON-state resistance of this transistor is a sum of a contact resistance (Rcnt) at an interface between the source electrode **708** and the n^+ source region **704**, a channel resistance (Rch) in the channel formed in the surface layer of the p base layer right below the gate electrode **707**, a JFET resistance (Rjfet) caused by narrowing of a current path due to the depletion layer, and a resistance (Rdrift) in the n drain drift region **702**.

In particular, the specific resistance and thickness of the n drain drift region **702** are important parameters for determining the withstand voltage of the element and the resistance (Rdrift) of the drift region **702**. In the structure shown in FIG. **7**(*a*), the optimum specific resistance and thickness of the n drain drift region **702** are determined depending upon the required level of the withstand voltage of the element, as described in A. S. Grove: Physics and Technology of Semiconductor Devices, John Wiley & Sons, p.197, FIG. 6.31, for example. Where the element is required to have a withstand voltage of 60V, the specific resistance and thickness of the n drain drift region **702** are 0.8 Ω·cm and 6.5 μm, respectively, and an effective thickness of the n epitaxial layer (Weff) that determines the withstand voltage is about 6 μm. The element withstand voltage, which is mainly determined by the structure as observed in the direction of depth of the element, is approximately equal to the withstand voltage of a diode including the p base region, n drain drift region **702** and the n^+ substrate **701** that are arranged in the depth direction of the element.

FIG. **8**(*a*) is a cross sectional view showing a principal part of another conventional MOSFET. This figure, like FIG. **7**(*a*), shows a unit cell of the MOSFET. In this unit cell, an n drain drift region (n epitaxial layer) **802** is laminated on an n^+ substrate **801**, to provide a semiconductor substrate. A p base layer **803** is formed in a surface layer of the semiconductor substrate, and a trench **805** is formed from the surface of the p base layer **803** to reach the n drain drift region **802**. An n^+ source region **804** is formed in a part of a surface layer of the p base layer **803**. A gate electrode **807** is disposed in the trench **805**, with a gate oxide film **806** interposed therebetween. A source electrode **808** is formed in contact with both the n^+ source region **804** and the p base region **803**, and a drain electrode **809** is formed on the rear surface of the n^+ substrate **801**. In operation of this element, when a positive voltage is applied to the gate electrode **807**, an n type inversion channel appears in a surface layer of the p base layer **803** beside the gate electrode **807**, whereby the n^+ source region **804** is conducted with the n drain drift region **802**. When the transistor is in its OFF state in which the gate voltage is not higher than a threshold level, on the other hand, the inversion channel is not formed in the surface of the p base layer **803**. In this state, the voltage applied to the transistor is carried by a depletion layer expanding over both sides of a pn junction between the p base layer **803** and the n drain drift region **802**.

FIG. **8**(*b*) is a view explaining details of the ON-state resistance of the power MOSFET of FIG. **8**(*a*). The ON-state resistance of this transistor is a sum of a contact resistance